INTERNSHIP OFFER - 4 to 6 months

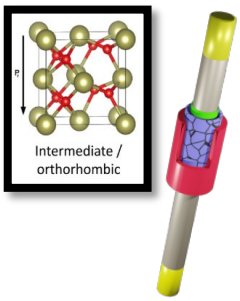
Understanding the electrical behavior of innovative vertically integrated nanoelectronic transistors

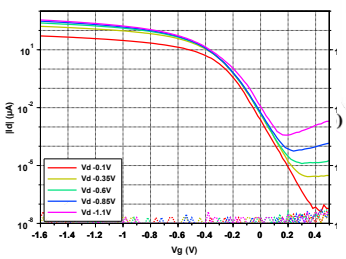
While artificial intelligence (AI) and machine learning techniques enjoy sustained interest across a broad range of application domains, current digital computing hardware is known to be inadequate to effectively implement AI, particularly in terms of energy efficiency. New technological breakthroughs at the device level are needed to enable the next AI revolutions with new forms of AI adapted to these technologies. Vertical gate-all-around nanowire field effect transistors, a disruptive technology where LAAS-CNRS is one of the world references, allows a truly 3D layout configuration to continue to scale gate length and benefit from scaling improvements to energy-efficiency. At the same time, over the last decade, the interest in the recently observed ferroelectric properties of doped hafnia and zirconia based materials has massively grown, thus giving a new perspective in the implementation of the latter in ultrascaled architectures for memory applications.
This internship is part of the **FVLLMONTI project** , which aim to explore high-performance and energy-efficient computing paradigms based on this vertical architecture as well as implementing a material with ferroelectric properties in the fabrication process. This will give the student a very stimulating context of **research collaboration in a multinational environment**.

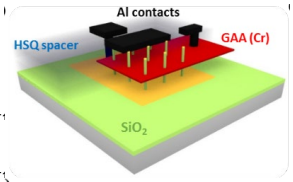
The intern will focus his work on the characterization of the novel non-conventional vertical transistor architecture devices and the implementation of the ferroelectric material as a memory element by getting involved in different stages of the procedure. This includes :

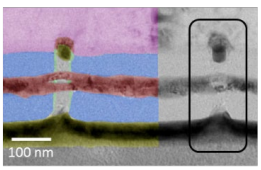
- Hands-on experience on the fabrication of ferroelectric devices.
- Electrical characterisation of Vertical gate-all-around nanowire field effect transistors and ferroelectric devices: connection with the physical parameters
- Manipulation of high-end equipment used in the technology research field.

The student will also gain theoretical knowledge on the operation vertical transistors as well as on ferroelectric materials for memory applications.









Work environment: The intern will be in the Nano&Neuro Electronics activity (within the MPN team) that has international recognition in the development of functional nano-devices for nanoelectronics applications.

Skills to be learned:

Multidisciplinary knowledge (nanoelectronics, applied physics, nanotech, device integration)
International collaboration in a multi – institutional European project

Ideal candidate:

- M1/M2 level or engineering student
- Enthusiastic and curious
- Background in Applied physics, Nanotechnology or Nanoelectronics
- Programming skills appreciated
- English level B2 or more

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